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TITLE: Test structure for measuring effect of **trench isolation** on oxide in a memory device

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TITLE - TI (1):
Test structure for measuring effect of **trench isolation** on oxide in a memory device

Brief Summary Text - BSTX (2):
The present invention relates to measuring effects of processes performed upon oxides in memory devices. More particularly, the present invention relates to a testing structure for measuring edge and corner effects of shallow **trench isolation** on tunnel oxides in a flash memory device.

Brief Summary Text - BSTX (4):
Advancements in technology and processes related to memory device fabrication have enabled continued scaling down (size reduction) of memory devices. As a memory device is scaled down, memory density is increased and the speed of the memory device is also increased. A contributory factor in the continuing scaling down of memory devices is the development of and introduction of **STI** (shallow **trench isolation**) into memory device fabrication.

Brief Summary Text - BSTX (5):
Implementing **STI** (shallow **trench isolation**) in memory device fabrication has enabled developers to properly scale down the memory device and improve circuit density. State of the art memory devices are being fabricated utilizing shallow **trench isolation** in the core memory area, realizing an improvement in memory density. Additionally, employing **STI** in memory device fabrication also maintains critical properties of a memory device, such as data retention, charge leakage, and device reliability under high voltage programming/erase operations.

Brief Summary Text - BSTX (6):
In memory device fabrication, one crucial process is the formation of the tunnel oxide. Tunnel oxide formation is closely coupled to **STI** related

processes. During the formation of **STI**, the silicon can be damaged at the **STI** corner (where the edges are compressed) and at the edge. **STI** damage is more severe at the corner due to compressed edges causing crystal disruption and/or crystal dislocation. This leads to imperfect tunnel oxide edge formation which can cause oxide edge degradation. Oxide edge degradation is a contributing factor in reliability, charge retention, and leakage problems in memory devices.

Brief Summary Text - BSTX (10):
Embodiments of the present invention are drawn to providing an apparatus and method for measuring effects of **isolation** processes, e.g., shallow **trench isolation**, on oxide formation, e.g., tunnel oxide in a memory device, e.g., a flash memory device. Embodiments of the present invention further provide an apparatus to provide more comprehensive measurements related to oxide formation. Embodiments of the present invention further provide an apparatus which includes corner characteristics in measurements related to oxide formation. Embodiments of the present invention additionally provide an apparatus that obtains those measurement in a simple manner and which is readily implemented during the fabrication of a memory device.

Detailed Description Text - DETX (2):
A method and apparatus for measuring effects of shallow **trench isolation** on oxide formation in a memory device. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the present invention.

Detailed Description Text - DETX (4):
The present invention, a test structure for measuring effects of **STI** (shallow **trench isolation**) on oxide formation in a memory device is described. In one example of one embodiment of the present invention, the memory device is a flash memory device. In one example of one embodiment, the oxide formed is tunnel oxide. However, it is noted that the present invention can be utilized to test almost any type of oxide formation, including gate oxide formation. Additionally, embodiments of the present invention are well suited for implementation in the fabrication of nearly all memory devices.

Detailed Description Text - DETX (7):
Referring to FIGS. 2A-2F collectively, cross-sectioned views of a memory

device, e.g., memory device 255a-f, during fabrication are shown. FIGS. 2A-2F are sequentially presented to illustrate processes performed during fabrication of a memory device prior to measuring a memory device to determine effects of **STI** (shallow **trench isolation**) on tunnel oxide formation in a memory device.

Detailed Description Text - DETX (10):
In FIG. 2C, processes associated with etching of nitride/mask layer 270 have been performed upon memory device 255b, resulting in a memory device 255c with an etched **STI** (shallow **trench isolation) trench** 280, as shown.

Detailed Description Text - DETX (11):
In FIG. 2D, processes associated with filling **STI** trench 280 of memory device 255c with an oxide have been performed upon memory device 255c, resulting in a memory device 255d with an oxide fill 285 in **STI** 280. It is noted that other processes, such as photoresist removal, liner oxidation, and densification of the oxide may have been performed in conjunction with the oxide fill.

Detailed Description Text - DETX (13):
In FIG. 2F, processes associated with cleaning and formation of a tunnel oxide layer have performed upon memory device 255e, resulting in a memory device 255f with a formed tunnel oxide layer 286, as shown. It is at this juncture in a process of fabricating memory device 255a-f that a testing for effects of **STI** (shallow **trench isolation**) on a tunnel oxide formation is conducted.

Detailed Description Text - DETX (14):
FIG. 3A is a block illustrated top/front-angled view of memory device 255f, analogous to memory device 255f of FIG. 2F. Memory device 255f shows a formed **STI** 280, an oxide fill 285, a source/drain region 250, and an oxide layer 286 (indicated with a dotted line). Formed **STI** 280 is shown to have an edge 263 and a corner 264. It is noted that there are four edges 263 and corners 264 within a formed **STI** 280. For purposes of the present disclosure, edges 263 will be considered as referring to all four edges 263 and corners 264 will be considered as referring to all four corners 264.

Detailed Description Text - DETX (15):
FIG. 3B is block illustrated top-view perspective of a memory device 255f, analogous to memory device 255f of FIG. 2F. Memory device 255f is shown having an sT 280, a source/drain region 250, a tunnel oxide 286 (indicated by dotted line), and a field area 130. In one embodiment, field **area** 130 is an **area of a test** structure 110, e.g., **test** structure 110b of FIG. 4B that encompasses

memory devices when disposed therein. Also shown are edge line 222e and corner line 222c. Edge line 222e indicates measurements of the electrical tests performed at edges 263 of **STI** 280 and corner line 222c indicates the measurements of electrical tests performed at corners 264 of **STI** 280 in memory device 255f. In one embodiment, the electrical tests can include, but are not limited to, capacitance-voltage tests, current-injection tests, and current-voltage tests. Accordingly, alternative tests can also be conducted upon memory device 255f.

Detailed Description Text - DETX (16):

Referring collectively to FIGS. 4A and 4B, a test structure 110a and a control test structure 110b are shown, respectively. Although thirty-five **STI** squares 281 and thirty-five **STI** circles 282 are shown in test structure 110a and control test structure 110b, respectively, a greater number or a lesser number of **STI** squares 281 or **STI** circles 282 can be disposed thereon.

Detailed Description Text - DETX (17):

FIG. 4A is a block illustration of a test structure 110, e.g., test structure 110a, in one embodiment of the present invention. In the present embodiment, test structure 110a is shown having an array of thirty-five **STI** squares 281. **STI** squares 281 are analogous to an **STI** 280 (as described in FIGS. 2C, 3A, and 3B) except that an **STI** square 281 is designed with the least design rules. **Test** structure 110a is also shown having a source/drain **region** 250 encompassing each **STI** 281. Measurements from electrical tests (described in FIG. 3B) conducted on each **STI** square 281 include measurements of corners 264 and edges 263, which are analyzed by tester/analyzer 120 coupled to test structure 110a (shown in FIGS. 1 and 5A).

Detailed Description Text - DETX (18):

FIG. 4B a block illustration of a control test structure 110, e.g., control test structure 110b, in one embodiment of the present invention. In the present embodiment, control test structure 110b is shown having an array of thirty-five **STI** circles 282. Control **test** structure 110b is also shown having a source/drain **region** 250 encompassing each **STI** circle 282. Control test structure 110b is adapted for utilization with test environment 100. **STI** circles 282 are analogous to an **STI** 280 (as described in FIGS. 2C, 3A, and 3B) except that an **STI** circle 282 is designed with the least design rules. It is noted that the perimeter of an **STI** circle 282 is equivalent to the perimeter of an **STI** square 281. Thus, measurements from electrical tests conducted on each **STI** circle 282 include perimeter values, but do not include corners 264, as no corners 264 are present in an **STI** circle 282.

Detailed Description Text - DETX (19):

Still referring collectively to FIGS. 4A and 4B, results of measurements of electrical tests conducted on **STI** circles 282 in control test structure 110b are then compared with results of measurements of electrical tests conducted on **STI** squares 281 in test structure 110a by tester/analyzer 120. By virtue of an **STI** circle 282 having a perimeter (edge) analogous to the edges 263 of an **STI** square 281, a difference in test results can therefore be attributed to corner damage incurred during formation of an **STI** 280. Corner damage includes silicon stress, crystal imperfections, crystalline dislocations, and the like. Further, corner damage is directly attributable to an imperfect tunnel oxide edge, causing oxide edge degradation. By providing an apparatus that incorporates corner measurements in the electrical tests conducted on memory devices, a more comprehensive evaluation of the memory device is realized.

Detailed Description Text - DETX (21):

FIG. 4C is a block illustration of a test structure 110, e.g., test structure 110c, in another embodiment of the present invention. In the present embodiment, test structure 110c is shown having an array of thirty-five memory devices 255r (analogous to memory device 255f of FIG. 2F) disposed therein. **Test** structure 110c is also shown having a field **area** 130 encompassing each memory device 255r. Measurements from electrical tests (described in FIG. 3B) conducted on each memory device 255r, including corners 264 and edges 263, are analyzed by tester/analyzer 120 coupled to test structure 110c (as shown in FIGS. 1 and 5A), and results are compared to results from tests conducted on control test structure 110d.

Detailed Description Text - DETX (22):

FIG. 4D is a block illustration of a control test structure 110, e.g., control test structure 110d, in another embodiment of the present invention. In the present embodiment, control test structure 110d is shown having an array of thirty-five circular memory devices 255s disposed therein. Control test structure 110d is adapted for utilization with test struture environment 100. Memory device 255s is analogous to memory device 255r of FIG. 4C and memory device 255f of FIGS. 2F, 3A, and 3B, except that it has a circular form, instead of rectangular. Control **test** structure 110d is also shown having a field **area** 130 encompassing each memory device 255s. It is noted that the perimeter of a memory device 255s is equivalent to the edges 263 of a memory device 255r. Thus, measurements from electrical tests conducted on each memory device 255s include perimeter values, but do not include corners 264, as no corners 264 are present in a memory device 255s. By virtue of measurements from electrical tests (described in FIG. 3B) conducted on each memory device 255f, including corners 264 and edges 263, are analyzed by tester/analyzer 120

coupled to test structure 110c (as shown in FIGS. 1 and 5A). The results are compared to an analogous control test structure 110d. A difference in the results of measurements of electrical tests obtained from the test structure 110c compared to the control test structure 110d results indicates imperfect tunnel oxide formation.

Detailed Description Text - DETX (23):

Still referring collectively to FIGS. 4C and 4D results of measurements of electrical tests conducted on memory devices 255s in control test structure 110d are then compared with results of measurements of electrical tests conducted on memory devices 255r in test structure 110c by tester/analyzer 120. By virtue of a memory device 255s having a perimeter (edge) analogous to the edges 263 of an memory device 255r, a difference in test results can therefore be attributed to corner damage incurred during formation of an **STI** 280. Corner damage includes silicon stress, crystal imperfections, crystalline dislocations, and the like. Further, corner damage is directly attributable to an imperfect tunnel oxide edge, causing oxide edge degradation. By providing an apparatus that incorporates corner measurements in the electrical tests conducted on memory devices, a more comprehensive evaluation of the memory device is realized.

Detailed Description Text - DETX (24):

By virtue of determining the condition of tunnel oxide prior to completion of fabrication of a memory device, the electrical test data can be utilized proactively to improve, alter, or readapt the fabrication process regarding the **STI** formation. One solution is that designers can implement a lighter **STI** formation or implement a stronger or lighter etch. Another solution is that designers can improve the design rule, such that the memory device is fabricated with rules for keeping a certain distance for the defect. Yet another solution is to improve the design itself, e.g., placing a layer of some material, (a nitride or alternative protecting material to prevent further degradation) on a corner of an edge, covering the entire memory device.

Detailed Description Text - DETX (26):

FIG. 5B is a block illustration of a plurality of test structures 110c, e.g., test structure 110c-1 and 110c-2, coupled with tester/analyzer 120. In FIG. 5B, each test structure contains an array of memory devices 255f, although in another implementation, each test structure can contain an array of **STIs** 280, as shown in FIG. 4A. Also shown are field **areas** 130, contacts 115, and a polysilicon layer covering both **test** structure 110c-1 and **test** structure 110c-2, as indicated by dotted line 116. FIG. 5B illustrates the flexibility of the present invention by showing that more than one test structure can be

electrically tested simultaneously. It is noted that additional test structures can be added, thus the number of test structures shown in FIG. 5B is exemplary and should not be construed as limiting. Additionally, simultaneous testing of arrays of 255f and/or arrays of 280s is an efficient and effective method of testing for tunnel oxide defects.

Detailed Description Text - DETX (27):
FIG. 6 is a flowchart 600 of steps performed in accordance with one embodiment of the present invention for measuring electrical tests to determine effects of **STI** on tunnel oxide in a memory device, e.g., a flash memory device. Flowchart 600 includes processes of the present invention which, in one embodiment, are carried out by an electrical testing and analyzing device, e.g., tester/analyzer 120 of FIG. 1. Although specific steps are disclosed in flowchart 600, such steps are exemplary. That is, the present invention is well suited to performing various other steps or variations of the steps recited in FIG. 6. Within the present embodiment, it should be appreciated that the steps of flowchart 600 may be performed by software, by hardware or by any combination of software and hardware.

Detailed Description Text - DETX (28):
In step 602 of FIG. 6, a memory device, e.g., a memory device 255 is being fabricated, as described in FIGS. 2A-2F. At the juncture as shown in FIG. 2F, memory device 255f is tested. Memory device 255f is arrayed in a test structure, e.g., memory device 255r in test structure 110c of FIG. 4C. Prior to testing, a layer of polysilicon is placed on top of test structure 110c, and contacts, e.g., contacts 115 are formed and then test structure 110c is coupled to a tester/analyzer, e.g., tester/analyzer unit 120 of FIG. 1, which then conducts various tests on memory devices 255r. It is noted that in another embodiment, test structure 110c can be comprised of **STIs** 282, as shown in test structure 110a in FIG. 4A. Electrical testing, in one embodiment, can include, but is not limited to, capacitance-voltage tests, current injection tests, and current-voltage tests.

Detailed Description Text - DETX (31):
In step 608 of FIG. 6, tester/analyzer unit 120 compares the results of the electrical tests conducted on test structure 110c with results of electrical tests conducted on a control test structure, e.g., control test stucture 110d. In the present embodiment, because the results of tests on control test structure menasurments rements are based on perimeter measurements (edge), and the results of measurements of electrical tests conducted on test structure 110c are based on measurements including edges 263 and corners 264, a difference between the two results indicated that the silicon was damaged

during the formation of an **STI**, e.g., **STI** 280 of FIG. 2C, resulting in an inperfect tunnel oxide. This can cause oxide edge degradation, thus causing realiability, charge retentention, and leakage problems in a memory device 255.

Detailed Description Text - DETX (32):

In conclusion, by providing more comprehensive data negarding certain electrical tests conducted on a memory device, e.g., a flash memory device, during its fabrication process, problems associated with damage and defects within the memory device, in particular during **STI** formation, can be reduced or eliminated, thus enabling fabrication of less problematic memory devices.

Claims Text - CLTX (1):

1. A method of evaluating an integrated circuit fabrication process comprising: performing an electrical **test on a test** structure comprising a first **region** having a polygon cross-section; measuring a parameter of said electrical test performed on said test structure; performing said electrical **test** on a control **test** structure comprising a second **region** having a circular cross section, wherein a perimeter of said circular cross section is substantially equal to a perimeter of said polygon cross-section; measuring said parameter of said electrical test performed on said control test structure; determining a corner effect on said parameter as a function of the difference between said measured parameter of said electric test performed on said test structure and said measured parameter of said electrical test performed on said control test structure.

Claims Text - CLTX (7):

7. An apparatus for evaluating a memory device comprising: a means for performing various electrical **tests** upon a **test** structure, wherein said **test** structure comprises a plurality of **regions** having edges and corners; means for collecting a first set of values regarding said various electrical tests conducted on said test structure; a means for performing various electrical **tests** upon a control **test** structure, wherein said control **test** structure comprises a plurality of **regions** having an edge and no corners and having a perimeter substantially equal or analogous to a perimeter of said **test** structure; means for collecting a second set of values regarding said various electrical tests conducted on said control test structure; and a means for generating data regarding a difference between said first set of values and said second set of values.

Claims Text - CLTX (9):

9. The apparatus according to claim 7, wherein said plurality of regions comprise shallow **trench isolation** regions.

Claims Text - CLTX (13):

13. An apparatus for evaluating a memory device fabrication process comprising: a **test** structure comprising an array of first **regions,** each having a corner, formed in a second **region**; a control **test** structure comprising an array of third **regions,** each not having said corner, formed in a forth **region,** wherein a perimeter of said array of third **regions** are substantially equal to a perimeter of said array of first **regions**; a test unit coupled to said test structure and to said control test structure, for performing an electrical test on said test structure and said control test structure; and an analyzer coupled to said test structure and to said control test structure, for determining a parameter as a function of said electrical test performed on said test structure and said control test structure.

Claims Text - CLTX (14):

14. The apparatus according to claim 13, wherein: said array of first regions comprise an array of shallow **trench isolation** regions; said second region comprises a source/drain region; said array of third regions comprise said array of shallow **trench isolation** regions; and said fourth region comprises said source/drain region.

Claims Text - CLTX (17):

17. The apparatus according to claim 13, wherein: said **test** structure further comprises a dielectric deposited upon said array of first **regions** and said second **region**; and said control **test** structure further comprises a dielectric deposited upon said array of third **regions** and said fourth **region**.